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<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Application Number	09/739,589
	Filing Date	12/15/00
	First Named Inventor	Steven Teig
	Group Art Unit	2825
	Examiner Name	A.M. Thompson
Total Number of Pages in This Submission	Attorney Docket Number	SPLX.P0014

Enclosures (Check all that apply)		
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Firm Or Individual name	Mani Adeli, Reg. No. 39,585 of Stattler Johansen & Adeli LLP
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Date	November 13, 2003

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PATENT  
Docket No. SPLX.P0014

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Mani Adeli

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig

Serial No.: 09/739,589

Filing Date: 12/15/00

For: METHOD AND APPARATUS FOR  
PRE-COMPUTING AND USING  
MULTIPLE PLACEMENT COST  
ATTRIBUTES TO QUANTIFY THE  
QUALITY OF A PLACEMENT  
CONFIGURATION WITHIN A  
PARTITIONED REGION

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INFORMATION DISCLOSURE  
STATEMENT UNDER 37 C.F.R. § 1.97

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11/19/2003 HGUTEMA1 00000034 09937589

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Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, applicants submit with this Information Disclosure Statement the attached Form PTO-1449, and copies of the documents listed in the 1449 form for consideration by the Examiner. The Examiner is requested to make these documents of record. Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

This Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is submitted after receipt of a first Office Action on the merits but before the Final Office Action. Accordingly, a fee is required. The requisite fee is attached.

However, in the unlikely event that the Patent Office determines that additional fees, extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 50-1128** referencing SPLX.P0014. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: November 13, 2003

Respectfully submitted,

By: \_\_\_\_\_

**Mani Adeli**

Registration No. 39,585

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<b>Substitute for form 1449A/PTO</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Application Number</b>	09/739,589
				<b>Filing Date</b>	12/15/00
				<b>First Named Inventor</b>	Steven Teig
				<b>Group Art Unit</b>	2825
				<b>Examiner Name</b>	A.M.Thompson
<b>Sheet</b>	1	of	7	<b>Attorney Docket Number</b>	SPLX.P0014

### U.S. PATENT DOCUMENTS

Examiner* Initials	Cite No. <sup>1</sup>	U.S. Patent Document		Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
	1.	2001/0009 031	A1	07-19-2001	Nitta et al.	
	2.	2002/0182 844	A1	12-05-2002	Igarashi et al.	
	3.	2003/0025 205	A1	02-06-2003	Shively	
	4.	2003/0005 399	A1	01-02-2003	Igarashi et al.	
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	7.	5,267,176		11-30-1993	Antreich et al.	
	8.	5,375,069		12-20-1994	Satoh et al.	
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	10.	5,618,744		04-08-1997	Suzuki et al.	
	11.	5,633,479		05-27-1997	Hirano	
	12.	5,637,920		06-10-1997	Loo	
	13.	5,640,327		06-17-1997	Ting	
	14.	5,663,891		09-02-1997	Bamji et al.	
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	18.	5,838,583		11-1998	Varadarajan et al.	
	19.	5,889,677		03-30-1999	Yasuda et al.	
	20.	5,980,093		11-09-1999	Jones et al.	

<b>Examiner Signature</b>		<b>Date Considered</b>	
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\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number(optional). <sup>2</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Application Number Filing Date First Named Inventor Group Art Unit Examiner Name				09/739,589	
				12/15/00	
				Steven Teig	
				2825	
				A.M.Thompson	
Sheet	2	of	7	Attorney Docket Number SPLX.P0014	

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	25.	6,295,634	B1	09-25-2001	Matsumoto	
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	41.	6,543,043	B1	04-01-2003	Wang et al.	
	42.	6,546,540	B1	04-08-2003	Igarashi et al.	
	43.	6,557,145	B2	04-29-2003	Boyle et al.	

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				<b>First Named Inventor</b>	Steven Teig
				<b>Group Art Unit</b>	2825
				<b>Examiner Name</b>	A.M.Thompson
<b>Sheet</b>	3	of	7	<b>Attorney Docket Number</b>	SPLX.P0014

U.S. PATENT DOCUMENTS					
	44.	6,567,967	B2	05-20-2003	Greidinger et al.

FOREIGN PATENT DOCUMENTS								
Examiner* Initials	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T 6
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code (if known)				
	45.	JP	411296560	A	Matsumoto et al.	10-29-1999	with English translation of Abstract;	
	46.	JP	2000-82743	A	Igarashi et al.	03-21-2000	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓
	47.	JP	H03-173471	A	Tawada et al.	07-26-1991	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓
	48.	JP	H05-243379	A	Masako Kubota	09-21-1993	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓
	49.	JP	H05-102305	A	Akihiro Sato	04-23-1993	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓

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				<b>Examiner Name</b>	A.M.Thompson
<b>Sheet</b>	4	of	7	<b>Attorney Docket Number</b>	SPLX.P0014

FOREIGN PATENT DOCUMENTS							
	50.	JP	H07-86407	A	Shinpei Miura	03-31-1995	with Japanese Patent Office's English translation of Abstract; and with English translation of the application. ✓
	51.	JP	H09-162279	A	Masaaki Yoshida	06-20-1997	with Japanese Patent Office's English translation of Abstract; and with English translation of the application. ✓

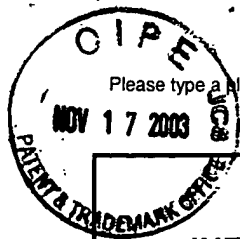
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				<b>Examiner Name</b>	A.M.Thompson
<b>Sheet</b>	5	of	7	<b>Attorney Docket Number</b>	SPLX.P0014

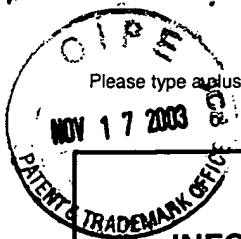
FOREIGN PATENT DOCUMENTS				
NON PATENT LITERATURE DOCUMENTS				
Examiner* Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 6	
	52.	Ahuja, R. et al., Faster Algorithms for the Shortest Path Problem, Journal of the Association for Computing Machinery, vol. 37, No. 2, April 1990, pp. 213-223.		
	53.	Brady, L. et al., Channel Routing on a 60° Grid, extended abstract, pp. 956-931.		
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	55.	Carothers, K., A Method of Measuring Nets Routability for MCM's General Area Routing Problems, 1999, pp. 186-192.		
	56.	Chen, H. et al., Physical Planning of On-Chip Interconnect Architectures, 2002, IEEE, International Conference, pp. 30-35.		
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	58.	Cheng, K., Steiner Problem in Octilinear Routing Model, a Thesis Submitted for the Degree of Master of Science, National University Singapore, 1995, pp. 1-122.		
	59.	Chip Model with Wiring Cost Map, August 1983, IBM Technical Disclosure Bulletin, vol. 26, iss. 3A, pp. 929-933.		
	60.	Cong, J. et al., Efficient Heuristics for the Minimum Shortest Path Steiner Arborescence Problem with Applications to VLSI Physical Design, Cadence Design Systems and UCLA Computer Science Department, pp.88-95.		
	61.	Cong, J. et al., Performance-Driven Multi-Layer General Routing for PCB/MCM Designs, UCLA Computer Science Department, 1998, pp. 356-361.		
	62.	Enbody, R. et al., Near-Optimal <i>n</i> -Layer Channel Routing, 23 <sup>rd</sup> Design Automation Conference, 1986, pp. 708-714.		
	63.	Fang, S. et al., Constrained Via Minimization with Practical Considerations for Multi-Layer VLSI/PCB Routing Problems, 28 <sup>th</sup> ACM/IEEE Design Automation Conference, 1991, pp. 60-65.		
	64.	Hom, I. et al., Estimation of the Number of Routing Layers and Total Wirelength in a PCB Through Wiring Distribution Analysis, 1996, pp. 1-6.		

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<b>Substitute for form 1449A/PTO</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Application Number</b>	09/739,589
				<b>Filing Date</b>	12/15/00
				<b>First Named Inventor</b>	Steven Teig
				<b>Group Art Unit</b>	2825
				<b>Examiner Name</b>	A.M.Thompson
<b>Sheet</b>	6	of	7	<b>Attorney Docket Number</b>	SPLX.P0014

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<b>Examiner Signature</b>		<b>Date Considered</b>	
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<b>Sheet</b>	7	of	7	<b>Attorney Docket Number</b>	SPLX.P0014

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